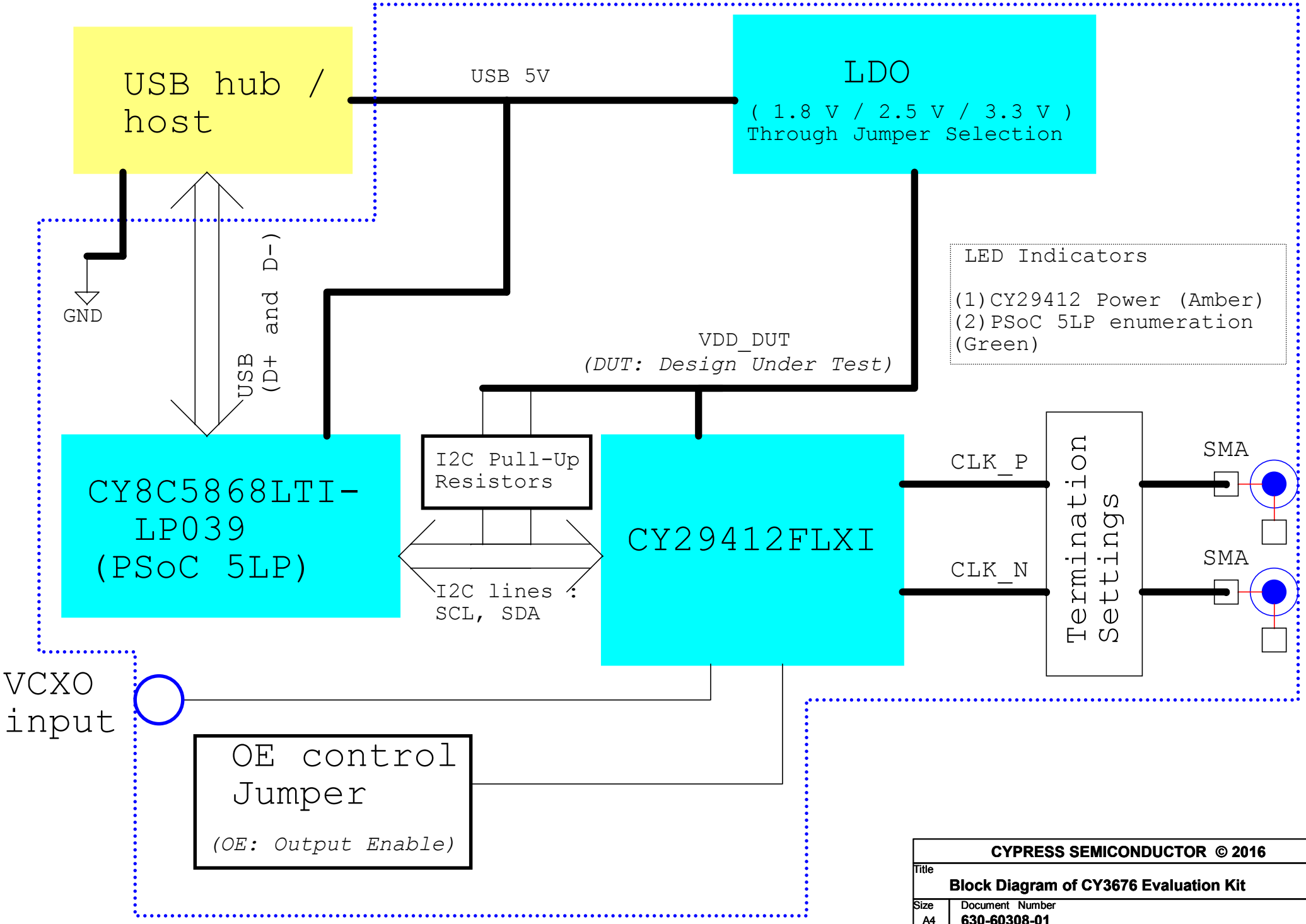


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| | | |
|---|---|---|
| Title | Block Diagram of CY3676 Evaluation Kit | |
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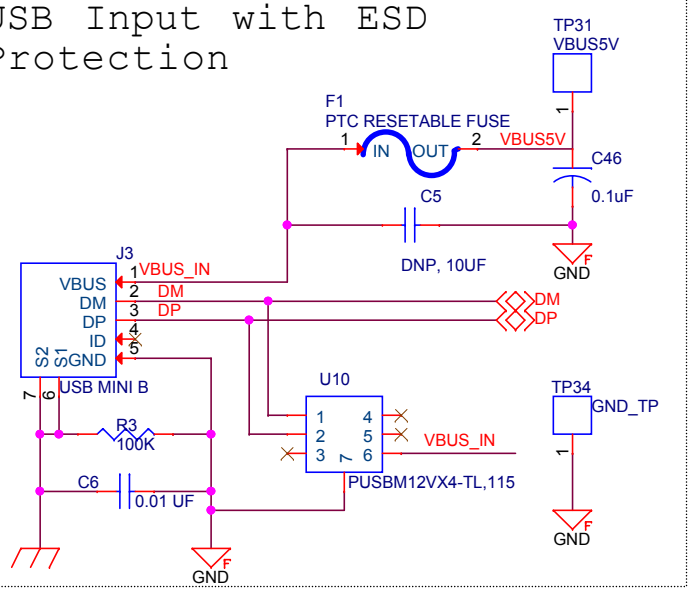
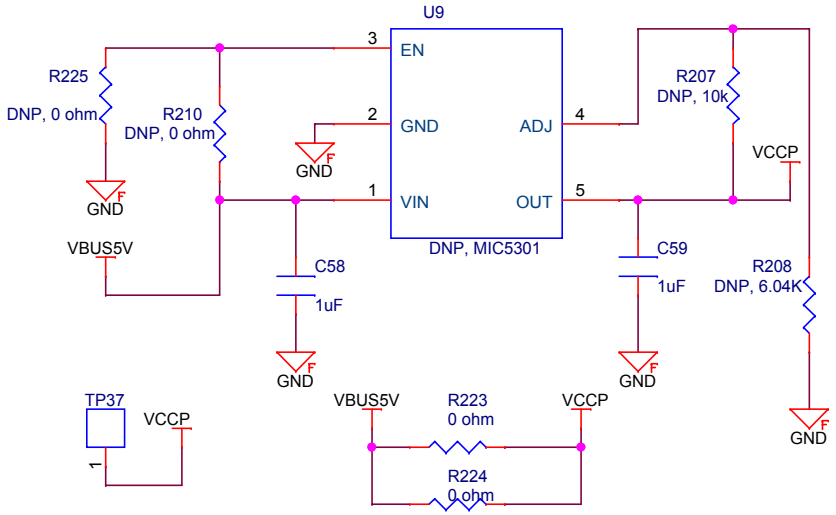
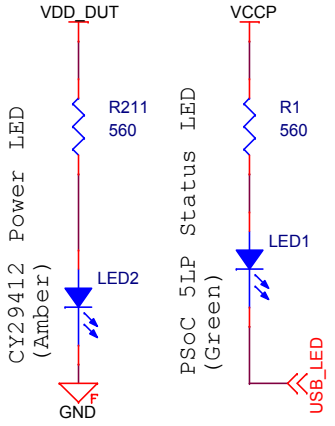
## USB Input with ESD Protection



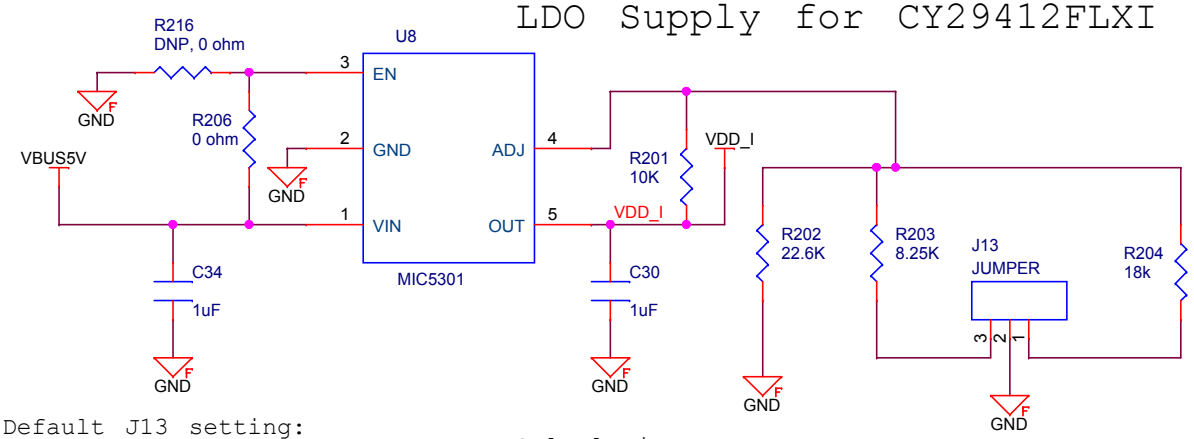

## Supply for PSoC 5LP




## Power and Status LEDs




## LDO Supply for CY29412FLXI




Default J13 setting:
Jumper shunt populated between pin 2 & 3

Note: The J13 jumper setting should match the Vdd profile created in ClockWizard.

| Jumper (J13) settings | VDD_I |
|---|---|
| Short 2 & 3 | 3.3V |
| Short 1 & 2 | 2.5V |
| Open | 1.8V |

Calculation:

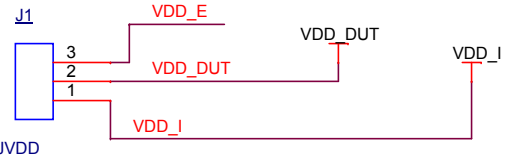
VREF = 1.25 V

Vout (i.e. "VDD_I") = VREF X ( 1 + R201 / Reff )

Reff = R202 : J13 open
= ( R202 || R203 ) : J13 short 2 and 3
= ( R202 || R204 ) : J13 short 2 and 1

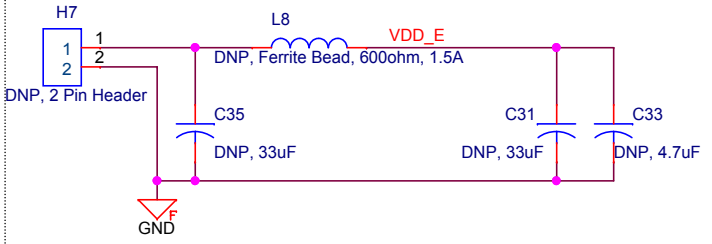
**Layout :Include this Table on the silk-screen top**

## Supply Jumper




Default :
Jumper shunt populated between pin 1 & 2

## Debug Point for CY29412




PCA : 121-60307-01 Rev 03
PCB : 600-60328-01 Rev 01
FAB DRW : 610-60302-01 Rev 01
ASSY DRW : 620-60310-01 Rev 01

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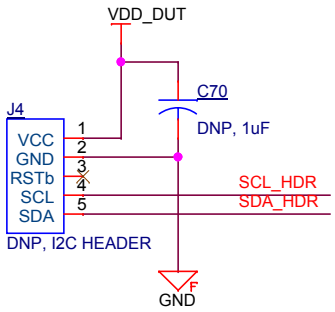
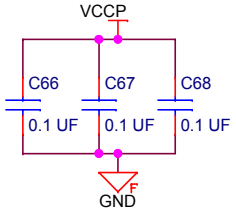
# PSoC 5LP Connections

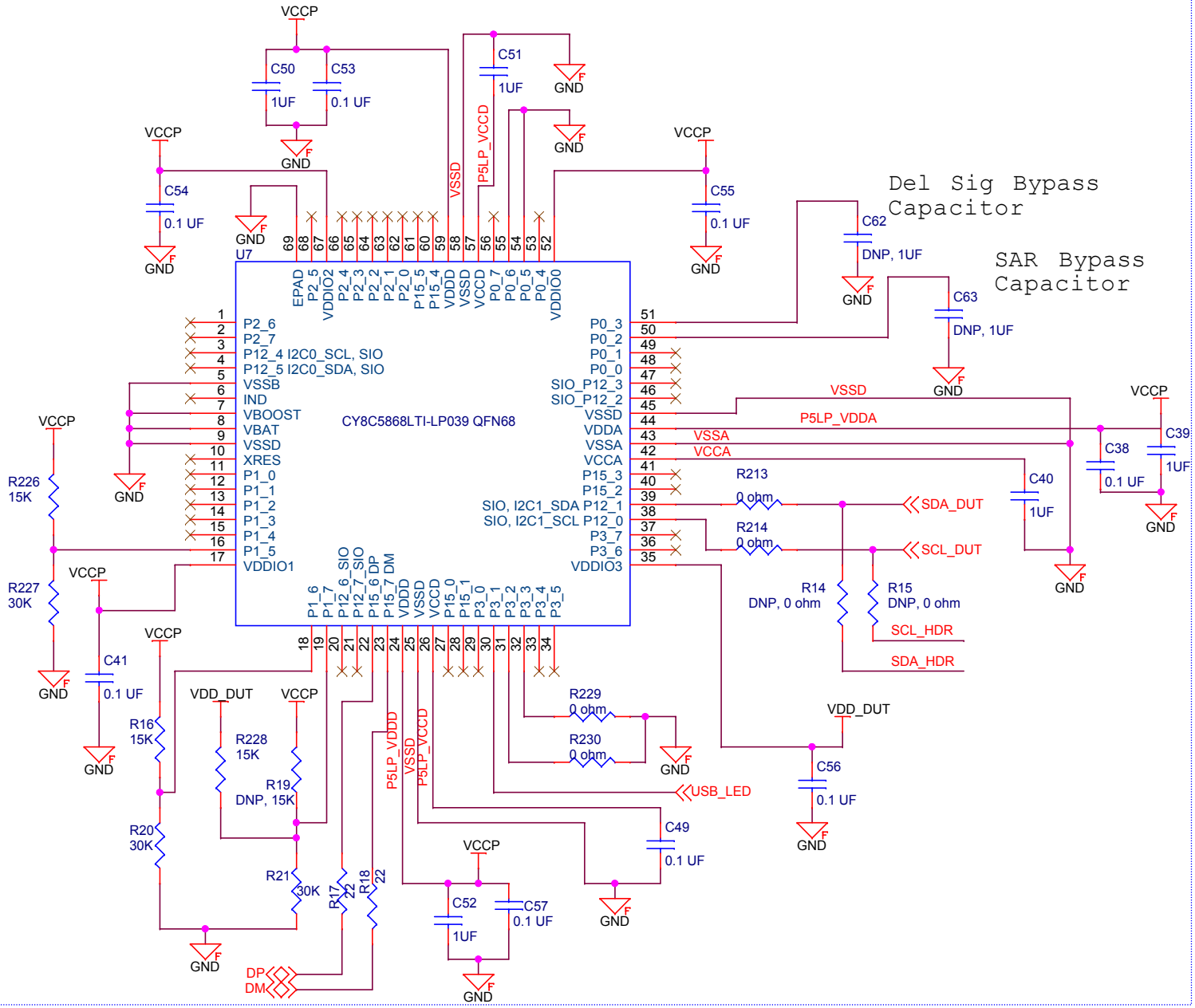
## 5-PIN I2C HEADER




J4 is DNP




Layout : (1) C67 to place close to pin U7.44, (2) C66, C68 to place close to pin U7.67

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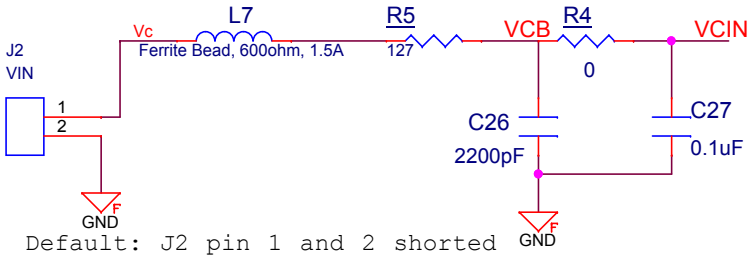
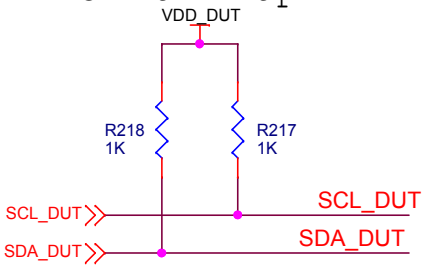
## Vcontrol Interface (VCXO)



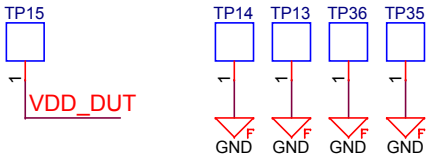

Default: J2 pin 1 and 2 shorted

Layout : This R-L-C filter should be placed very close to the IC pin U1.1

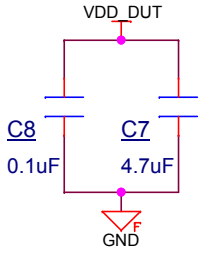
## I2C Pull up




Layout : SCL_DUT and SDA_DUT recommended be equal length (length matched)

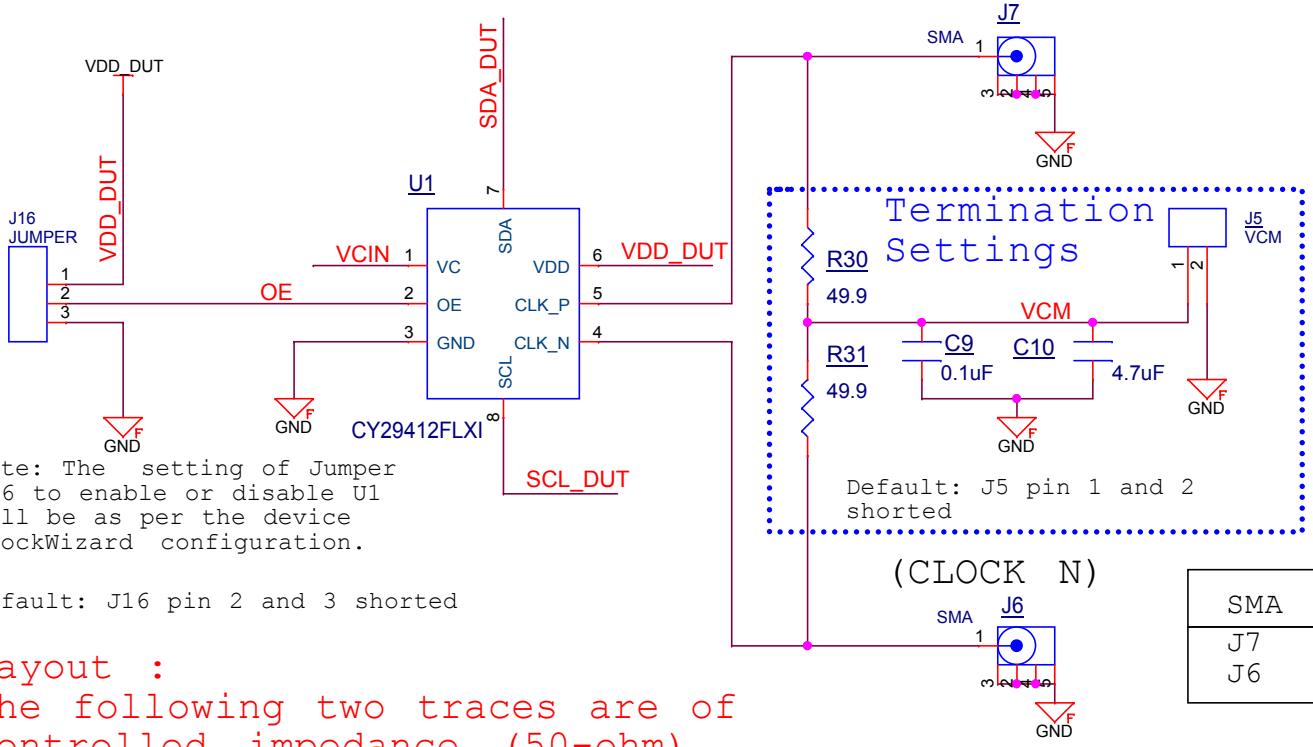



Layout : Test Points Spread around U1 IC




Layout : Decaps should be placed close to U1 Supply and Ground pins

## CY29412FLXI Interface




Note: The setting of Jumper J16 to enable or disable U1 will be as per the device ClockWizard configuration.

Default: J16 pin 2 and 3 shorted

Default: J5 pin 1 and 2 shorted

| SMA | FUNCTION |
|---|---|
| J7 | CLK_P |
| J6 | CLK_N |

Layout :
The following two traces are of controlled impedance (50-ohm).
(1) Trace connecting U1.5 and J7.1,
(2) Trace connecting U1.4 and J6.1,

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